SN75161B, SN75162B
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

SLLS005B – OCTOBER 1980 – REVISED MAY 1995

- **Meets IEEE Standard 488-1978 (GPIB)**
- **8-Channel Bidirectional Transceivers**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **Designed to Implement Control Bus Interface**
- **SN75161B Designed for Single Controller**
- **SN75162B Designed for Multiple Controllers**
- **High-Speed, Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 72 mW Max Per Channel**
- **Fast Propagation Times . . . 22 ns Max**
- **High-Impedance pnp Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Bus-Terminating Resistors Provided on Driver Outputs**
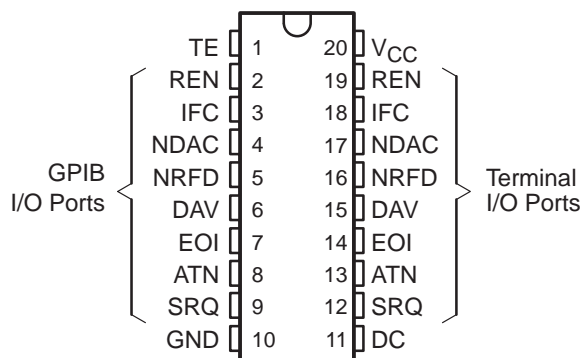- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**

description

The SN75161B and SN75162B eight-channel, general-purpose interface bus transceivers are monolithic, high-speed, low-power Schottky devices designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a single- or multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75161B or SN75162B provides the complete 16-wire interface for the IEEE-488 bus.

The SN75161B and SN75162B feature eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. A power-up/-down disable circuit is included on all bus and receiver outputs. This provides glitch-free operation during V_{CC} power up and power down.
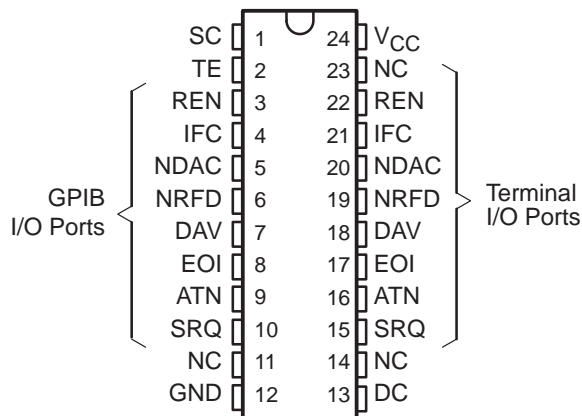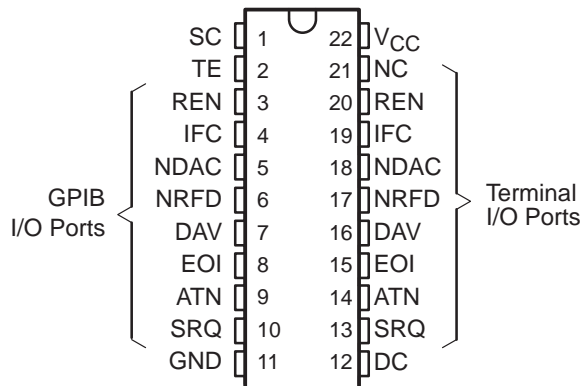
SN75161B . . . DW OR N PACKAGE
(TOP VIEW)

GPIB I/O Ports	Pin	#	#	Pin	Terminal I/O Ports
	TE	1	20	V_{CC}	
	REN	2	19	REN	
	IFC	3	18	IFC	
	NDAC	4	17	NDAC	
	NRFD	5	16	NRFD	
	DAV	6	15	DAV	
	EOI	7	14	EOI	
	ATN	8	13	ATN	
	SRQ	9	12	SRQ	
	GND	10	11	DC	

SN75162B . . . DW PACKAGE
(TOP VIEW)

GPIB I/O Ports	Pin	#	#	Pin	Terminal I/O Ports
	SC	1	24	V_{CC}	
	TE	2	23	NC	
	REN	3	22	REN	
	IFC	4	21	IFC	
	NDAC	5	20	NDAC	
	NRFD	6	19	NRFD	
	DAV	7	18	DAV	
	EOI	8	17	EOI	
	ATN	9	16	ATN	
	SRQ	10	15	SRQ	
	NC	11	14	NC	
	GND	12	13	DC	

SN75162B . . . N PACKAGE
(TOP VIEW)

GPIB I/O Ports	Pin	#	#	Pin	Terminal I/O Ports
	SC	1	22	V_{CC}	
	TE	2	21	NC	
	REN	3	20	REN	
	IFC	4	19	IFC	
	NDAC	5	18	NDAC	
	NRFD	6	17	NRFD	
	DAV	7	16	DAV	
	EOI	8	15	EOI	
	ATN	9	14	ATN	
	SRQ	10	13	SRQ	
	GND	11	12	DC	

NC – No internal connection

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SN75161B, SN75162B
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

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description (continued)

The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC (on SN75162B) enable signals. The SC input on the SN75162B allows the REN and IFC transceivers to be controlled independently.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75161B and SN75162B are characterized for operation from 0°C to 70°C.

Function Tables

SN75161B RECEIVE/TRANSMIT

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(Controlled by DC)					(Controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

H = high level, L = low level, R = receive, T = transmit, X = irrelevant
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side.
Data transfer is noninverting in both directions.
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

SN75162B RECEIVE/TRANSMIT

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
				(Controlled by DC)		(Controlled by SC)			(Controlled by TE)		
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

H = high level, L = low level, R = receive, T = transmit, X = irrelevant
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side.
Data transfer is noninverting in both directions.
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

CHANNEL-IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	
TE	Talk Enable	Control
SC	System Control (SN75162B only)	
ATN	Attention	
SRQ	Service Request	
REN	Remote Enable	Bus
IFC	Interface Clear	Management
EOI	End of Identity	
DAV	Data Valid	
NDAC	Not Data Accepted	Data
NRFD	Not Ready for Data	Transfer

SN75161B logic symbol†
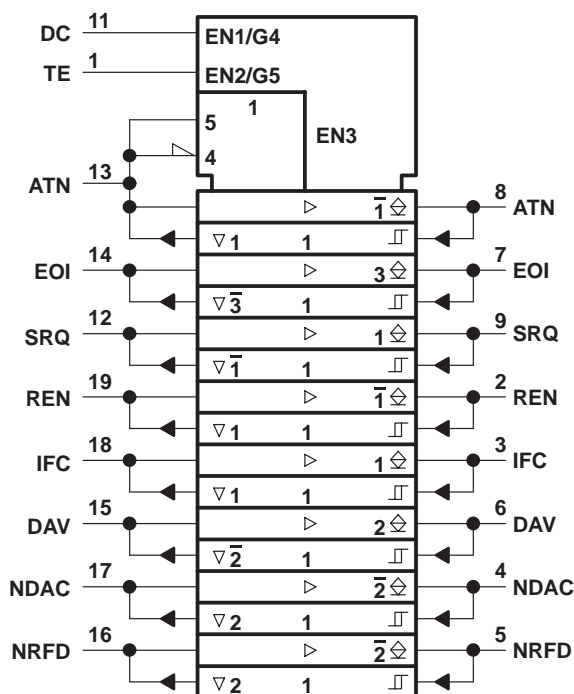
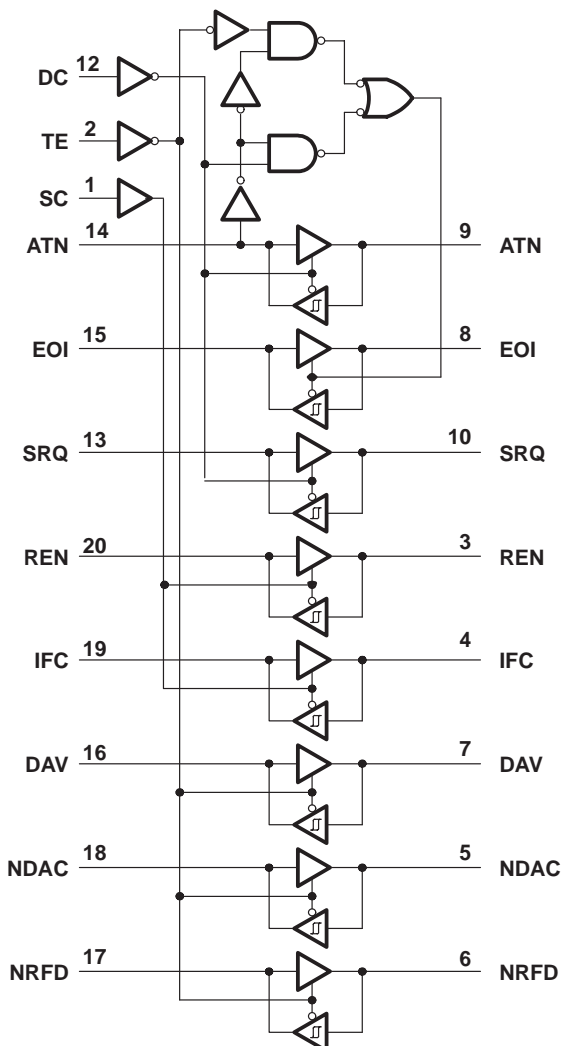## SN75161B logic diagram (positive logic)
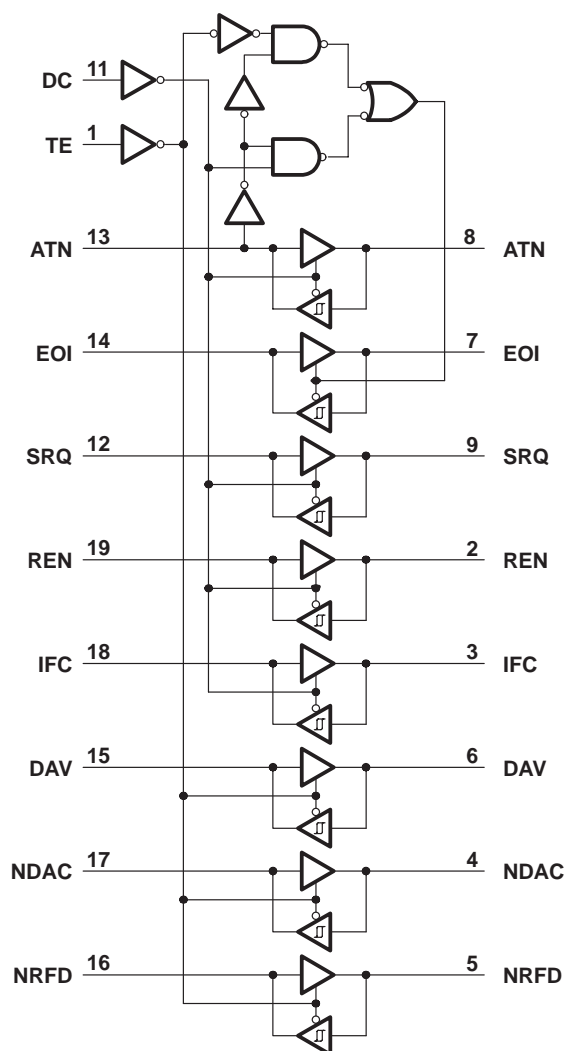
† This symbol is in accordance with IEEE Std 91-1984 and
IEC Publication 617-12.

▽ Designates 3-state outputs

⇔ Designates passive-pullup outputs

SN75162B logic symbol†
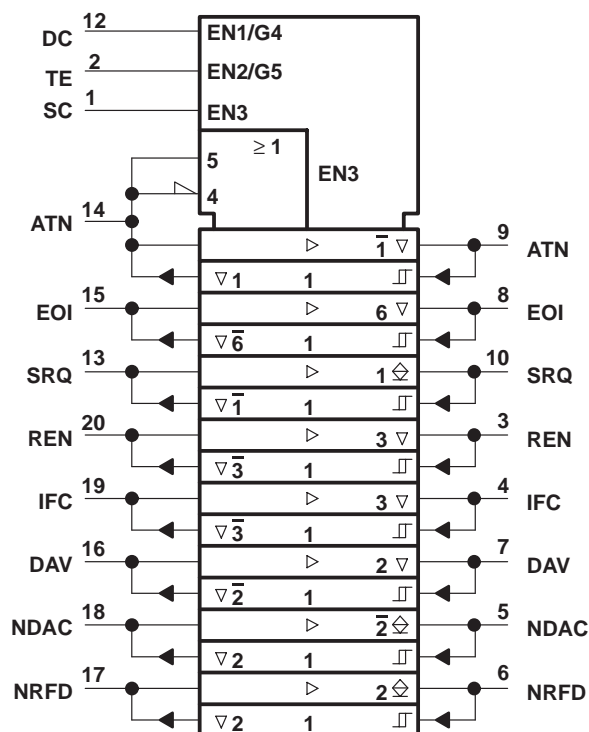
†This symbol is in accordance with IEEE Std 91-1984 and
IEC Publication 617-12.
▽ Designates 3-state outputs
⇪ Designates passive-pullup outputs
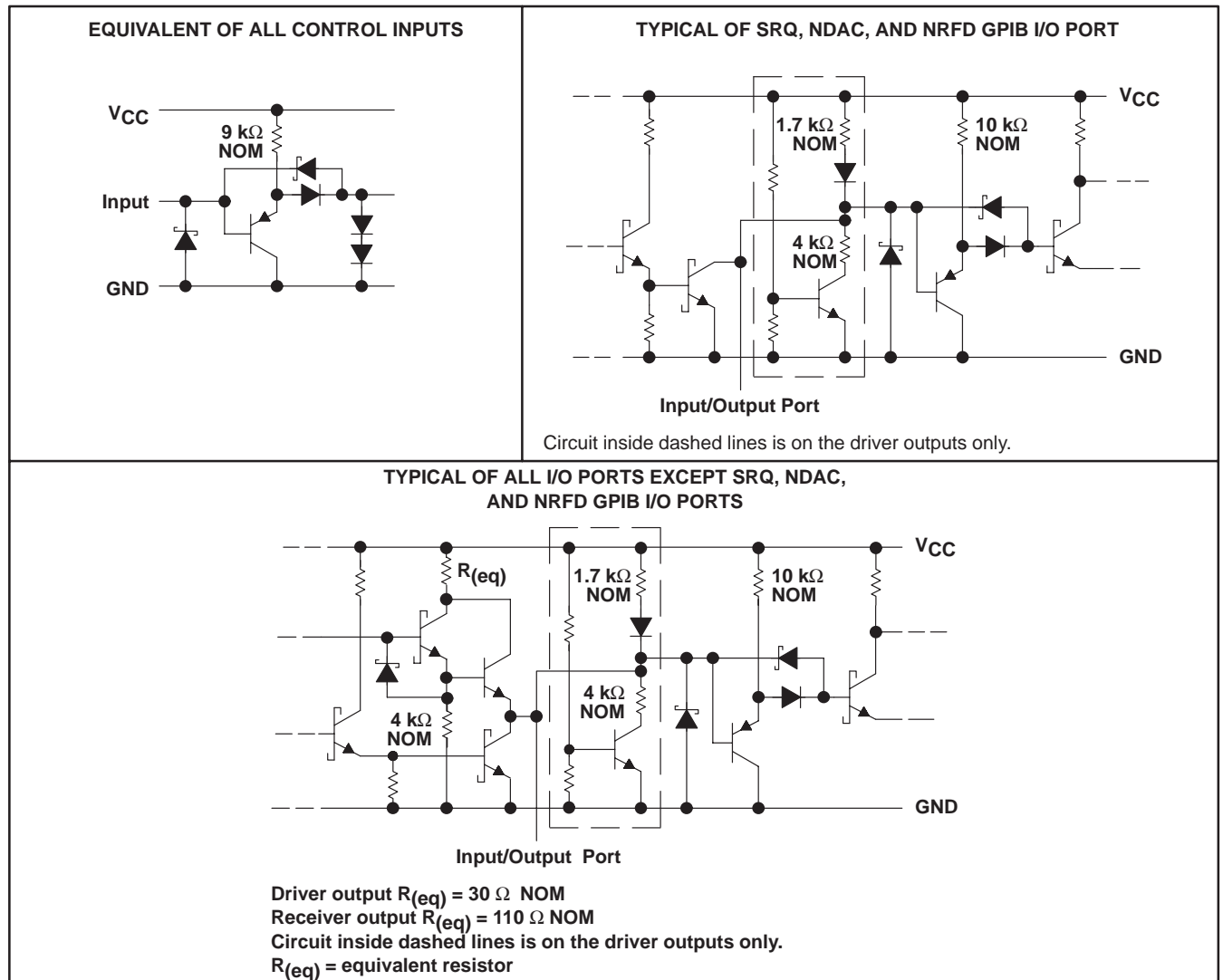
SN75162B logic diagram (positive logic)

Pin numbers shown are for the N package.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

TYPICAL OF SRQ, NDAC, AND NRFD GPIB I/O PORT

Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC,
AND NRFD GPIB I/O PORTS

Input/Output Port

Driver output $R_{(eq)}$ = 30 Ω NOM
Receiver output $R_{(eq)}$ = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.
$R_{(eq)}$ = equivalent resistor

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage, V_I . . . . 5.5 V
Low-level driver output current, I_{OL} . . . . 100 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1:   All voltage values are with respect to network ground terminal.

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DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW (20 pin)	1125 mW	9.0 mW/°C	720 mW
DW (24 pin)	1350 mW	10.8 mW/°C	864 mW
N (20 pin)	1150 mW	9.2 mW/°C	736 mW
N (22 pin)	1700 mW	13.6 mW/°C	1088 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -18$ mA			-0.8	-1.5	V
V_{hys}	Hysteresis voltage $(V_{IT+} - V_{IT-})$	Bus	See Figure 7		0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	$I_{OH} = -800$ µA		2.7	3.5		V
		Bus	$I_{OH} = -5.2$ mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	$I_{OL} = 16$ mA			0.3	0.5	V
		Bus	$I_{OL} = 48$ mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	$V_I = 5.5$ V			0.2	100	µA
I_{IH}	High-level input current	Terminal and control inputs	$V_I = 2.7$ V			0.1	20	µA
I_{IL}	Low-level input current		$V_I = 0.5$ V			-10	-100	µA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)} = 0$	2.5	3.0	3.7	V
				$I_{I(bus)} = -12$ mA			-1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)} = -1.5$ V to 0.4 V	-1.3			mA
				$V_{I(bus)} = 0.4$ V to 2.5 V	0		-3.2	
				$V_{I(bus)} = 2.5$ V to 3.7 V			2.5	
							-3.2	
				$V_{I(bus)} = 3.7$ V to 5 V	0		2.5	
				$V_{I(bus)} = 5$ V to 5.5 V	0.7		2.5	
		Power off	$V_{CC} = 0$,	$V_{I(bus)} = 0$ V to 2.5 V			-40	µA
I_{OS}	Short-circuit output current	Terminal			-15	-35	-75	mA
		Bus			-25	-50	-125	
I_{CC}	Supply current		No load, TE, DE, and SC low				110	mA
$C_{I/O(bus)}$	Bus-port capacitance		$V_{CC} = 5$ V to 0, $V_{I/O} = 0$ to 2 V, f = 1 MHz			16		pF

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ V_{OH} applies for 3-state outputs only.

SN75161B, SN75162B
## OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					14	20	
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus (SRQ, NDAC, NRFD)	C_L = 30 pF, See Figure 1		29	35	ns
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					15	22	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Bus (ATN, EOI, REN, IFC, and DAV)	See Figure 3			60	ns
t_{PHZ}	Output disable time from high level						45	
t_{PZL}	Output enable time to low level						60	
t_{PLZ}	Output disable time from low level						55	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	See Figure 4			55	ns
t_{PHZ}	Output disable time from high level						50	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						55	
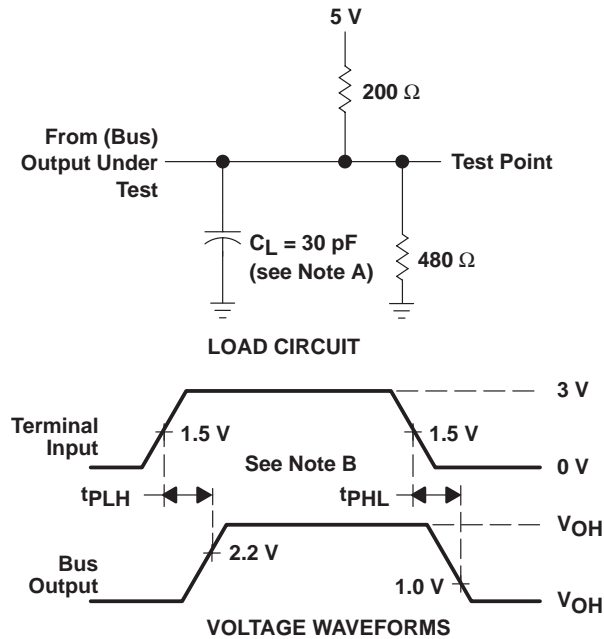
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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

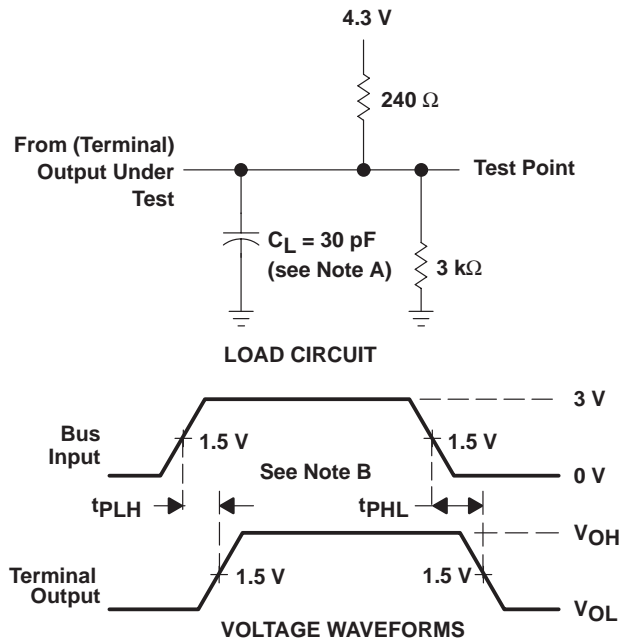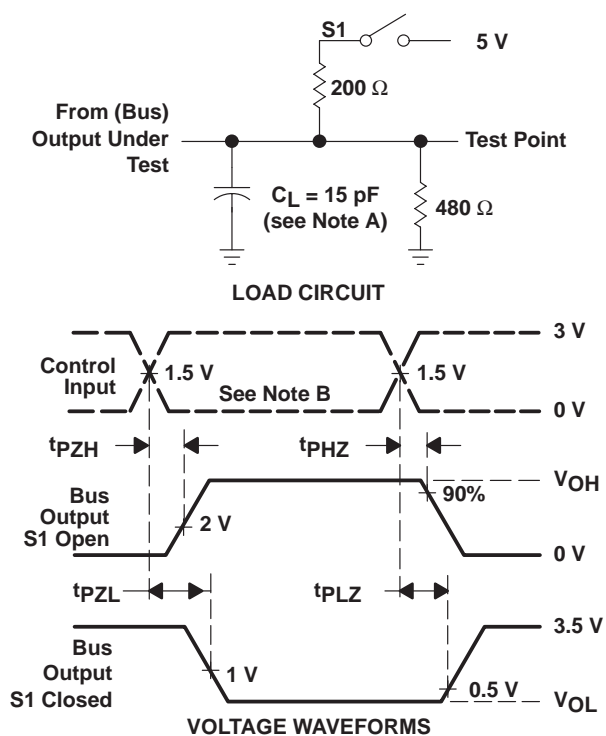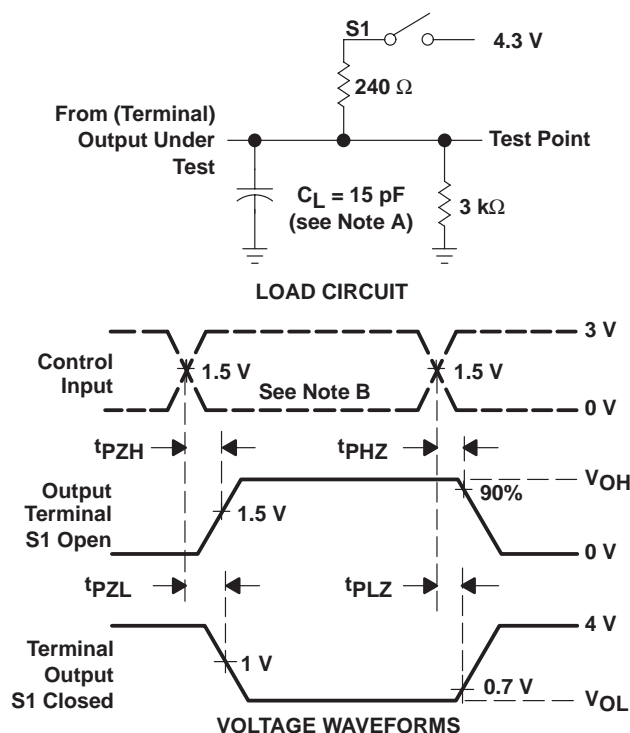**VOLTAGE WAVEFORMS**

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

LOAD CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 3. Bus Enable and Disable Times Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

VOLTAGE WAVEFORMS

Figure 4. Terminal Enable and Disable Times Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
        B. The Input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL I/O PORTS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

$V_{CC} = 5$ V
$T_A = 25°C$

Figure 5

TERMINAL I/O PORTS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

$V_{CC} = 5$ V
$T_A = 25°C$

Figure 6

TERMINAL I/O PORTS
OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

$V_{CC} = 5$ V
No Load
$T_A = 25°C$

V_{IT-} V_{IT+}

Figure 7

TYPICAL CHARACTERISTICS

**GPIB I/O PORTS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

Figure 8

**GPIB I/O PORTS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

Figure 9

**GPIB I/O PORTS
OUTPUT VOLTAGE
vs
THERMAL INPUT VOLTAGE**

Figure 10

**GPIB I/O PORTS
CURRENT
vs
VOLTAGE**

Figure 11

PACKAGE OPTION ADDENDUM
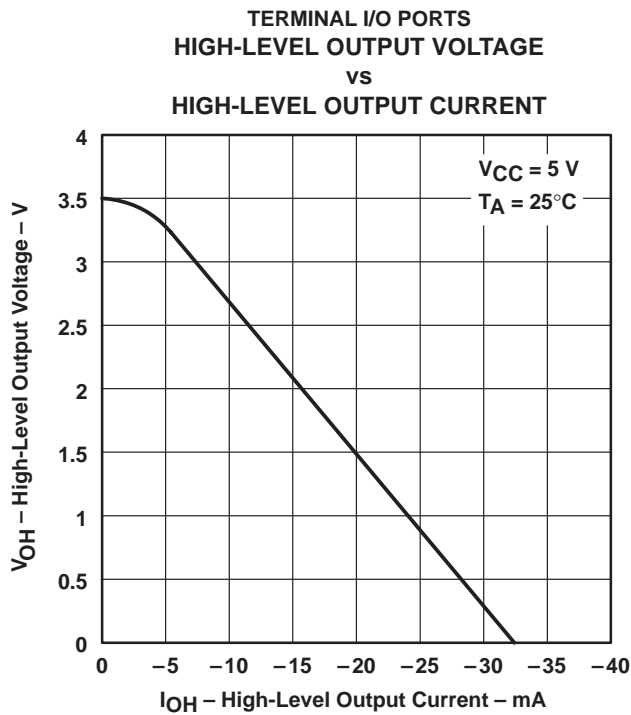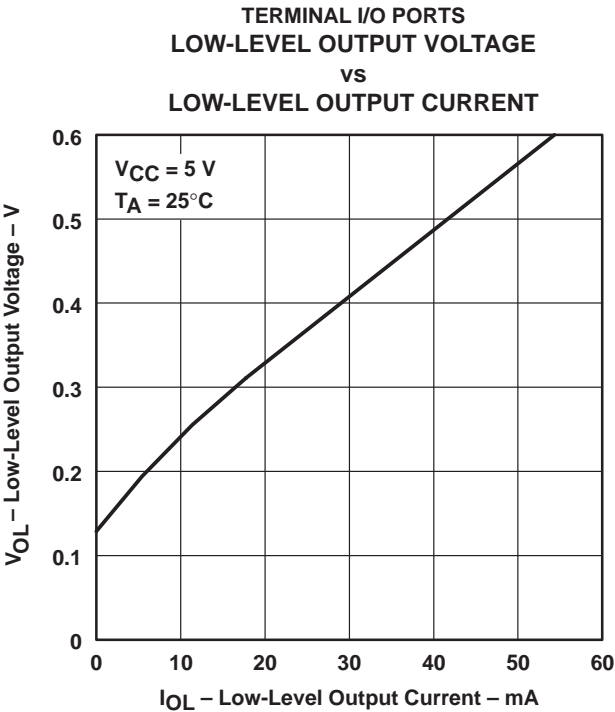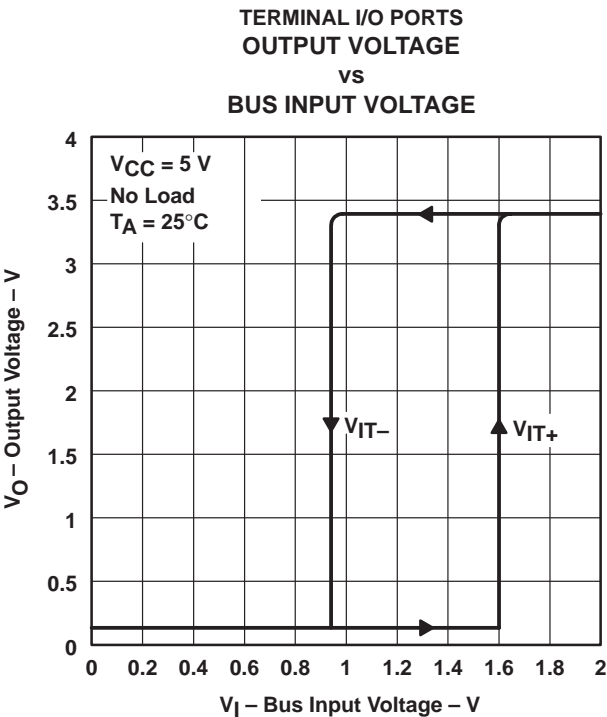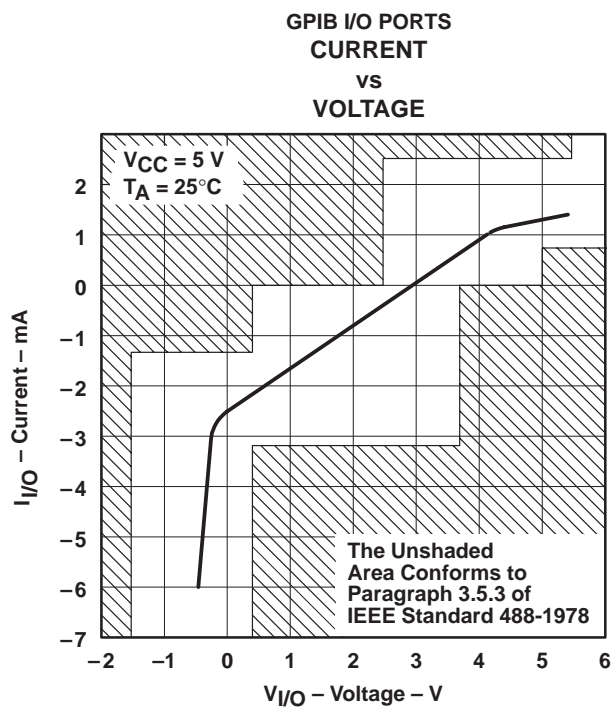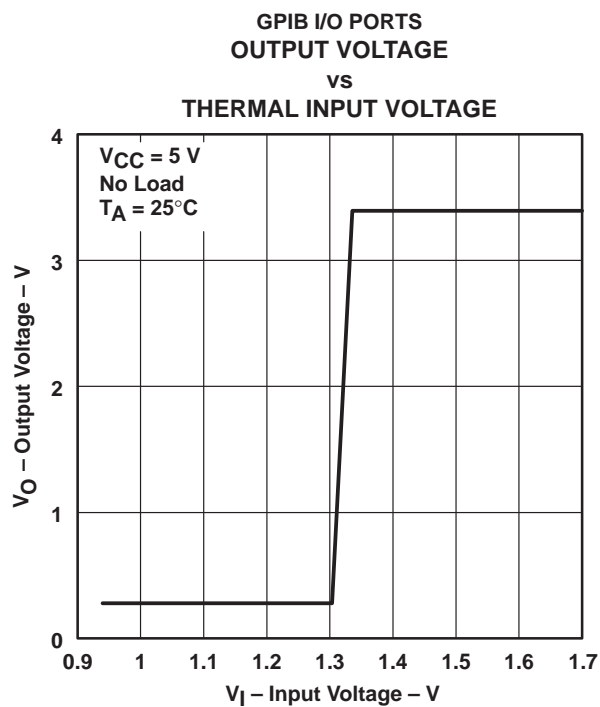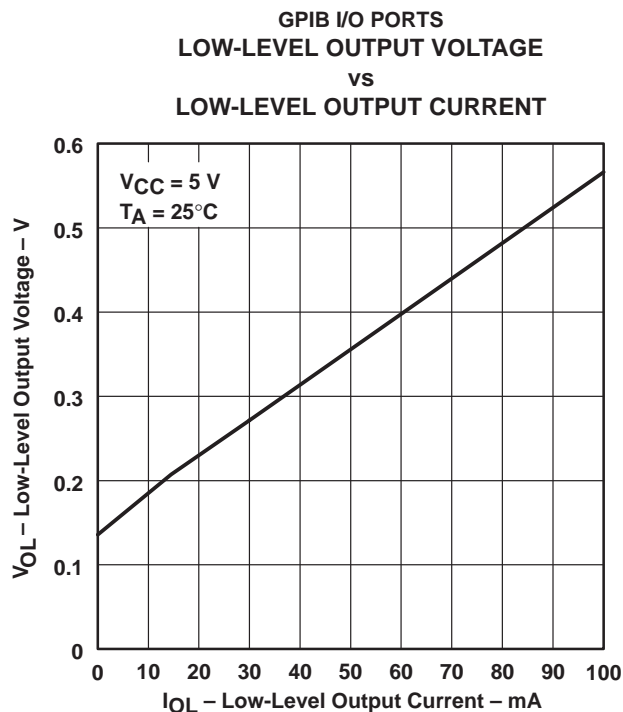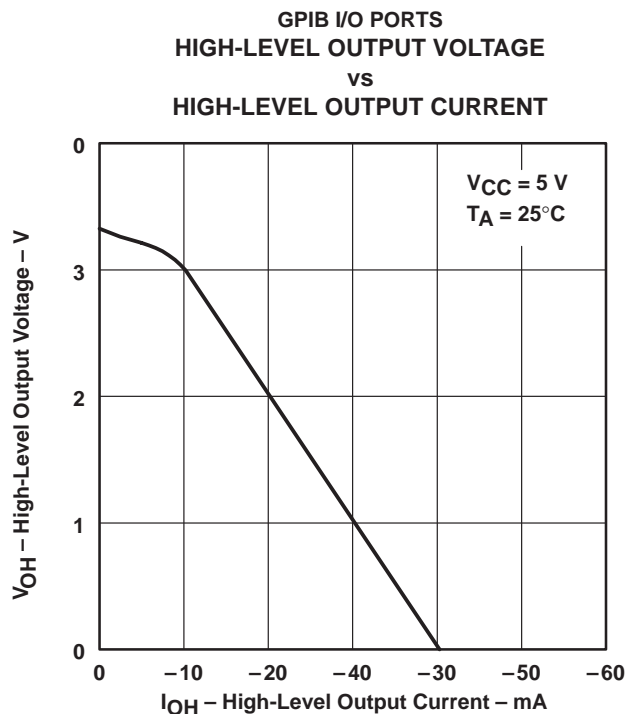
PACKAGING INFORMATION

Orderable Device (1)	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75161BDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B	Samples
SN75161BDWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B	Samples
SN75161BDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B	Samples
SN75161BDWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B	Samples
SN75161BDWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75161B	Samples
SN75161BN	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75161BN	Samples
SN75161BNE4	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75161BN	Samples
SN75162BDW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75162B	Samples
SN75162BDWE4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75162B	Samples
SN75162BDWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75162B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75161BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75162BDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75161BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75162BDWR	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

0.614 (15,60)
0.598 (15,20)

24   13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⌖ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−5/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
          D.   Falls within JEDEC MS−013 variation AD.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) △D

0.045 (1,14) / 0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         △C   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         △D   The 20 pin end lead shoulder width is a vendor option, either half or full width.

10.63 / 9.97 TYP

A

PIN 1 ID AREA

1

18X 1.27

20

13.0 / 12.6 NOTE 3

2X 11.43

10

11

7.6 / 7.4 NOTE 4

B

20X 0.51 / 0.31

⊕ | 0.25Ⓜ | C | A | B

C

SEATING PLANE

⌒ | 0.1 | C

2.65 MAX

0.33 / 0.10 TYP

SEE DETAIL A

0.25 GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL
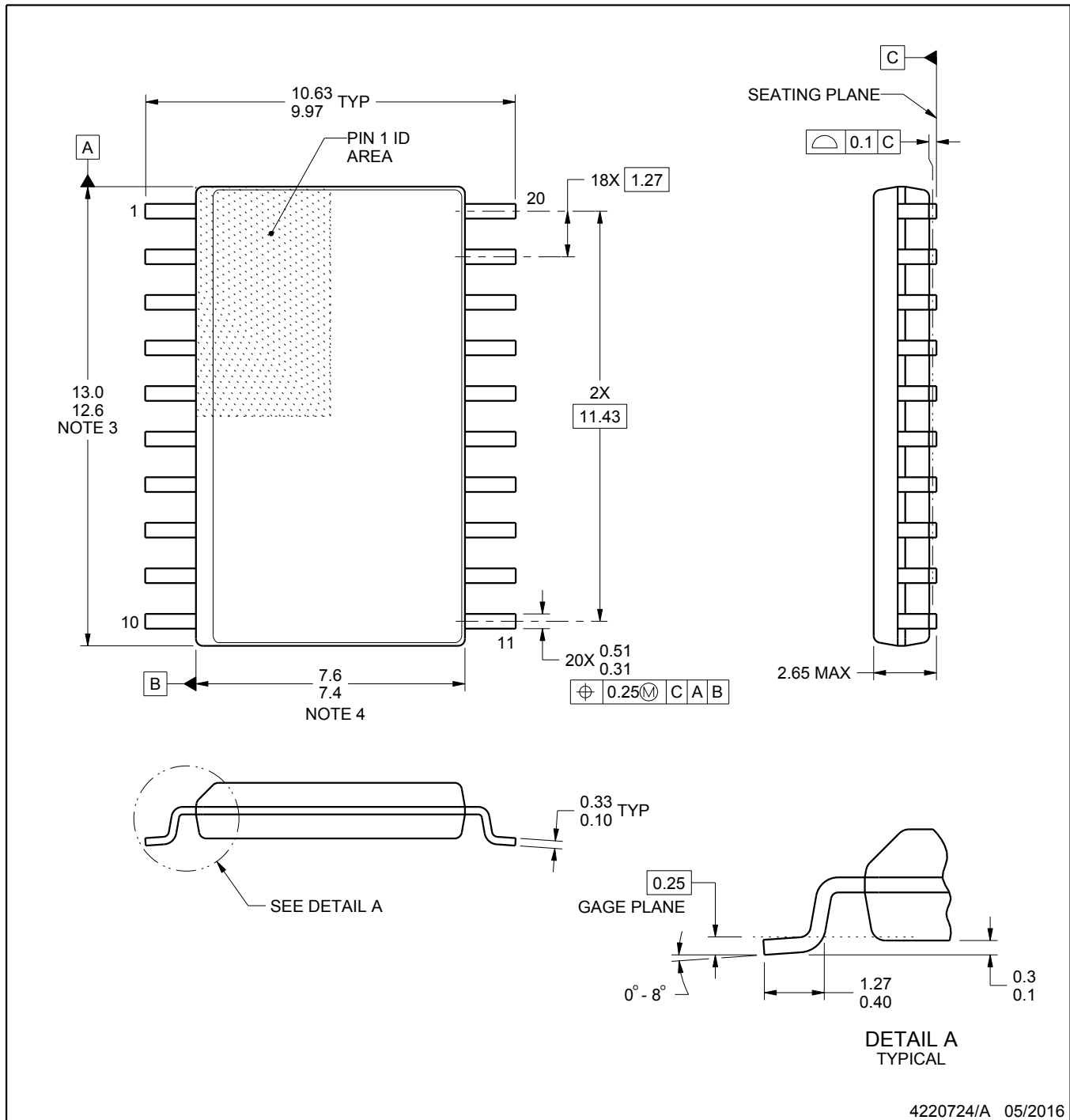
4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

TEXAS INSTRUMENTS
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20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
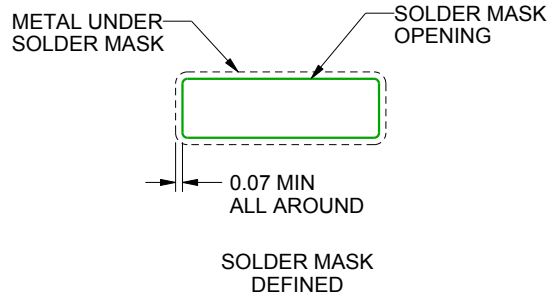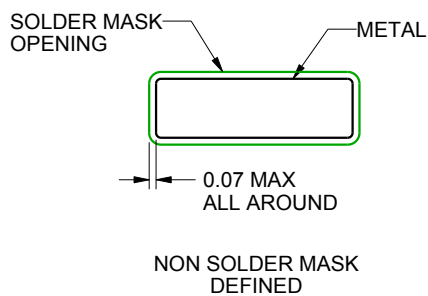
SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.